AMENDMENTS TO THE SPECIFICATION

Please amend the title appearing on the cover sheet and on pages 1 and 41 of the application as follows:

METHODS AND SYSTEMS FOR MAINTAINING INFORMATION FOR LOCATING NON-NATIVE PROCESSOR INSTRUCTIONS WHEN EXECUTING NATIVE PROCESSOR INSTRUCTIONS

Please amend the paragraph starting at line 4 on page 11 as follows:

The ACPC register 61 and the Here register 62 can be distinguished from each other at least by their respective functions. For example, the ACPC register 61 points where to resume execution after a rollback, in other words the last place at which a commit operation was performed. The ACPC register 61 points to an ~~a the~~ address of a native instruction. The Here register 62 points to a native code point from which the PC, IP or other information about a translation can be recovered from, or where "rollback compensation" is performed (rollback compensation is described further below). These and other features and functions of the ACPC and Here registers will become fully evident in the discussions to follow.

Please amend the paragraph starting at line 4 on page 22 as follows:

The first instruction (molecule) in subroutine 140 is VLIW 136, which includes pre-atom 138. It is important to note that native instructions other than native instructions 133 can execute a call for subroutine 140. Each of these ~~These~~ other native instructions will have its own commit, and each will have its own distinct EIP.

Please amend the paragraph starting at line 11 on page 31 as follows:

In step 730, when the exception is taken, an address in a register is read. In one embodiment, the address in the Here register 62 (Figure 1B) is read. In such an embodiment, the address in the Here register 62 will point to one of the native instructions in the translation. As described above, that instruction will include a number of bits, including an indicator bit (e.g., third bit 113 of Figure 2B) and a plurality of pointer bits (e.g., pointer bits 114 of Figure 2B). In step 740, depending ~~Depending~~ on the value of the indicator bit, the EIP of interest can be directly recovered or rollback compensation is implemented. In other words, depending on the value of the indicator bit, the pointer bits will point either to the EIP of interest, or to other information (e.g., another instruction or a subroutine) that can be used for recovering the EIP of interest.